ESSOR HDR BASE WF – METHODOLOGY AND RESULTS FOR DEVELOPING A PORTABLE COALITION WAVEFORM SOFTWARE

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ABSTRACT

The ESSOR HDR Base WF is the common portable software jointly developed by the ESSOR stakeholders in order to be ported on different heterogeneous national SDR platforms. As such, this is a significant result of ESSOR.

After presenting the summary of the key capabilities of the ESSOR HDRWF, this paper details: (i) the ESSOR Methodology for Portability, a generic methodology elaborated to design and validate the Base WF, and relying on the ESSOR Architecture; (ii) the application of this methodology to the development of the HDR Base WF, with its reference structure; (iii) the concepts, architectural implications and uses of the Native Test Environment specifically developed for incrementally validating the HDR Base WF; (iv) the results of current incremental porting activities of the HDR Base WF on the heterogonous national SDR Platforms, with the initial lessons learnt.

1. INTRODUCTION

The European Secure SOftware defined Radio (ESSOR) Programme is a major Software Defined Radio (SDR) program established under the umbrella of the European Defense Agency (EDA)[1], sponsored by the governments of Finland, France, Italy, Poland, Spain and Sweden. ESSOR has been awarded by the Organisation Conjointe de Coopération en matière d'ARmement (OCCAR) [2] to the joint venture Alliance for ESSOR (a4ESSOR S.A.S.) in charge of managing the industrial consortium composed of the following respective National Champions (NC): Elektrobit, THALES Communications & Security, SELEX ES, RADMOR, Indra and Saab AB.
Along with the definition and implementation of the ESSOR Architecture [3], an SDR architecture extending the public part of the JTNC [4] Software Communications Architecture (SCA) [5], ESSOR specifies, simulates and designs the ESSOR HDRWF (High Data Rate WaveForm), develops this WF as a shared and portable software application (the HDR Base WF), ports this shared WF application on heterogeneous national SDR platforms (PTF), and finally demonstrates interoperability amongst these PTFs.

After summarizing the HDRWF key capabilities (§2), this paper presents the motivation for developing a Base WF, the ESSOR Methodology for Portability and its relationship with the ESSOR Architecture (§3), provides the application of this methodology to the development of the ESSOR HDR Base WF and details its structure (§4), explains the HDR Base WF validation process (§5), provides status of HDR Base WF porting on national SDR Platforms (§6), and finally concludes with perspectives on future steps (§7).

2. HDRWF CAPABILITIES & ARCHITECTURE

This section summarizes the key capabilities and architecture of the HDRWF, a coalition secure high data rate mobile ad hoc networking waveform for land military applications. A more in-depth description of the operational aspects and concepts of use of the HDRWF can be found in the paper presented at MILCOM'13, [6].

2.1. HDRWF Key Capabilities

The HDRWF capabilities have been defined in order to sustain an evolutionally development path. In the current phase of the programme: (i) Threshold Capabilities (T) refer to features that are subject to detailed design, simulation, software development, porting and interoperability testing; (ii) Objective Capabilities (O) refer to features that are studied up to WF architecture definition, giving confidence

that WF architectural foundations are sound to support a full development of the capabilities inside future activities.

A. MANET and Synchronization

HDRWF is a multi-hop mobile ad-hoc network (MANET), supporting up to 200 nodes per network, communication on the move (up to 130 km/h) and dynamic adaptation to the environment (propagation, topology, node density, advantaged nodes, traffic profile). Each node is acting as transmitter, receiver or relay and allows interconnection with IP networks. The distributed and secured synchronization mechanisms operate with and without GNSS, utilizing GNSS even when partially available. In that case, all nodes are synchronizing on the reduced set of nodes with GNSS. After splitting, network partitions run autonomously, but merging or node late entry is always possible since adequate mission parameters are shared by the nodes. Depending on frequency resources available, multiple ESSOR networks can coexist on the battlefield.

B. Remote and Local Management

HDRWF network provides local and remote management capabilities. Local management, using the Human Machine Interface (HMI) of each node, provides administrative functions to the local operator, such as loading of mission parameters, supervision and control of node behaviour, radio silence (O), group joining/leaving, power on/off, display of information, notification (e.g. faults reports and retrieval of collected logs). Remote management, using Network Management System (NMS), provides administrative functions similar to local management and allows for flexible integration of the HDRWF NMS into existing national infrastructures. Using SNMPv3 [7], the NMS can also perform Over the Air (OTA) management on the data defined in Management Information Base (MIB).

C. IP Based Services

The HDRWF supports IPv4 simultaneously unicast, optimized multicast and broadcast communications for IP-voice, data (Blue force tracking, FTP), and video traffic with different Quality of Services (QoS). Integration of IPv6, header compression, QoS-based routing and time critical transmission are foreseen for future steps (O).

D. Voice Services

The HDRWF voice services include VoIP [8] and embedded Combat Net Radio (CNR) voice Push To Talk (PTT) (O), where voice (and other low latency) traffic are given preferential treatment over other services.

E. Spectrum and Signal in Space

HDRWF Signal in Space (SiS) operates in UHF band (225-400 MHz) with a 1.25 MHz channel bandwidth, a good compromise between waveform performance and spectrum allocation. SiS provides three data rates (~1 Mbps, ~ 512 and ~ 256 kbps) at radio link, dynamically selected according to channel conditions and/or transmission needs, operates with TRANSEC based frequency-hopping as Anti-Jamming (AJ) and frequency diversity technique, and uses improved AJ solutions to protect communication, like interference cancellation and self-interference avoidance in the presence of high-altitude nodes.

F. Information Assurance

HDRWF Information Assurance objectives are to provide Confidentiality, Integrity, Availability and Accountability to the network, the users and their assets; withstanding and mitigating the potential threats in the tactical operational environment. This is achieved by the means of embedded communication security (COMSEC), network security (NETSEC) and transmission security (TRANSEC).

2.2. HDRWF Architecture

Fig. 1 illustrates the HDRWF logical stack organized around the Networking (NET), Link Layer Control (LLC), Medium Access Control (MAC), Physical (PHY), and Management (MGT) layers. This modular architecture enables incremental development in front of future capabilities.
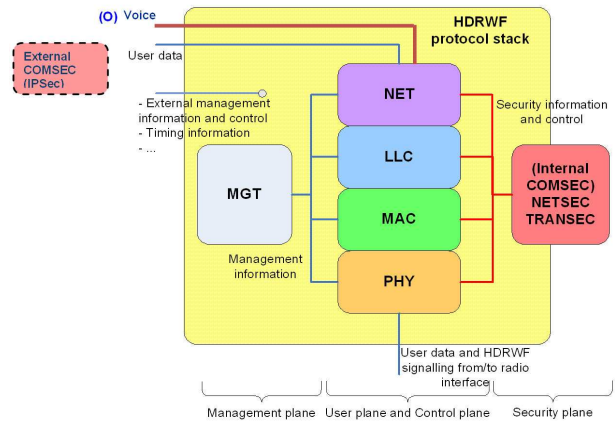

Fig. 1. HDRWF Layers Decomposition

NET layer adapts received IP packets from upper layers and dispatches them in the HDRWF network. Destination IP address is mapped to the MAC address and some information from the IP header (e.g.: Addresses, Differential Services Coding Point (DSCP) [9], etc.) is used for flow classification. Route discovery and maintenance in the internal addressing plan is performed using a customized version of OLSR [10] proactive link state protocol.
LLC layer performs traffic shaping by the means of Segmentation and Reassembly (SAR) and management of priority queues for different IP traffic according to its DSCP

value, giving preferential treatment for low latency traffic and high priority services. LLC also supports high reliability traffic by a tailored Automatic Repeat Request (ARQ) mechanism (hop by hop).

MAC layer provides a synchronized TDMA scheme to dynamically share the transmission medium with multiple physical channels. MAC manages synchronization according to time reference locally available at node level (GNSS), or exchanged through the network.

PHY layer provides the means of transmitting bit streams (user data and signalling data) over the radio link, performing modulation, demodulation, synchronization, dwell management, TRANSEC protection and transceiver.

MGT Layer controls the entire HDRWF logical stack state machine (including remote/local deactivation and re-initialization of the node). It realizes all functionalities for local and remote management and manages parameters (as e.g. routing table) and security material (as e.g. keys, certificates).

3. ESSOR METHODOLOGY FOR WF PORTABILITY

With the goal to **improve Interoperability** through the use of **Coalition waveforms,** ESSOR has recognized the benefit **to share common WF software** (**the HDR Base WF)** amongst the industrial and governmental stakeholders, providing the ability to **bound national investments** and use **common interoperability references.** Taking into account the intrinsic **diversity of the national SDR Platforms**, the **ESSOR Methodology for WF Portability and the HDR Base WF** are at the core of this approach.

The HDRWF development and validation steps (TABLE I) are organized in order to give assurance on the waveform performance, to support joint development of the HDR Base WF software amongst the ESSOR stakeholders, and to give confidence on the porting of the HDR Base WF on the various and heterogonous national SDR Platforms (PTFs).

TABLE I. HDRWF DEVELOPMENT AND VALIDATION STEPS

HDRWF Development Steps	HDRWF Validation Steps
HDRWF System Design	High Fidelity (HiFi) Simulations
HDR Base WF Software Development	Native Test Environment (NTE)
HDRWF ported on National SDR PTF	National Test Bed (*)
Interoperability Labs Tests	Multinational Test Bed (MTB)

- (*) National Test Bed is duplicated / extended from the MTB

3.1 Overview of ESSOR Methodology
The ESSOR Methodology for WF Portability was defined in a generic way prior its application for the ESSOR HDR WF development. The whole methodology relies on the fundamental assumption that **Target Waveforms** are executing on SDR platforms after the **porting** of a common development basis named the **Base Waveform**, developed in a highly portable fashion and validated within a **Native Test Environment**, as depicted in Fig.2:
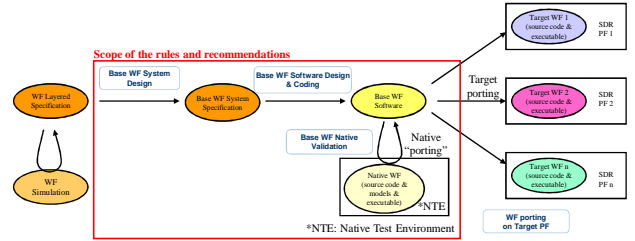

Fig. 2. Overview of ESSOR methodology scope

4 main steps are identified by the methodology:
- Base WF System Design,
- Base WF Software Design,
- Base WF Software Coding,
- Base WF Native Validation.

3.2. Base WF System Design

Base Waveform System Design is the **first** phase of Base WF development. It essentially consists in designing: (i) the functional components of the Base WF, denoted as **Base Software Items** (**BSIs**), (ii) their **requirements towards the functional support** (Radio Devices (RD), Radio Services (RS) and Radio Security Services (RSS) and their performance criteria) of any hosting platform.

This phase decomposes in **three activities**: **WF/PF separation**, **Base WF partitioning** and **Base WF mapping**.

It can be supported by UML/SysML modeling, the methodology having defined a **WF PIM modeling language profile** for that purpose.

3.2.1 WF / PF separation

The entry point of this activity is **one *entire* waveform (capability)**, that encompasses **the complete functional behavior** of a radio executing the considered waveform, that is assumed to be specified into a *WF Layered Specification* (set of Layer Specifications for the considered waveform).

The purpose of **WF / PF separation** is to **separate each Layer** in two parts: (i) the functionalities assigned to the **base waveform**, to be implemented in **portable software**, and (ii) the **functional support**, to be implemented by **any SDR platform executing the considered waveform**.

The interfaces between **base waveform** and **functional support** (RD, RS, RSS) are determined by a set of

functional APIs that need to belong to a SDR standard such as the ESSOR Architecture. In addition to only specifying software interfaces, **performance criteria** (as identified in ESSOR Architecture) are an essential enabler for specification of the **performance requirements** applying to the *functional support* that the platform is to deliver.

The ESSOR methodology is not limited to Base WF software aspects, in asking for exhaustive and consistent specification of the *functional support* Base WF relies on. Usage of SDR standards where functional performance criteria are associated to APIs software interfaces is one essential enabler for such specification.

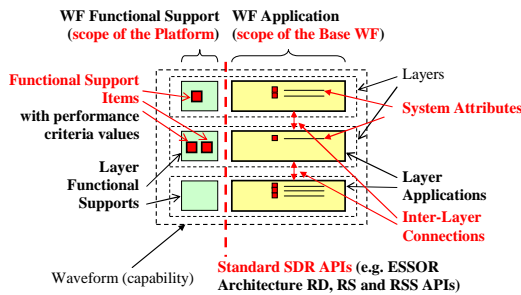Fig. 3 illustrates the outcome of WF/PF separation:

Fig. 3. Illustrative outcome of WF/PF separation

3.2.2 Base WF partitioning

The entry point of this activity is the set **of Layer Applications** as identified by previous activity.

The purpose of **Base WF partitioning** is to **decompose each Layer Application** into functional components named Base Software Items (BSIs). While BSIs are specified **independently from any *explicit* assumptions** regarding implementation choices, they need to be **small enough** to be portable on Processing Element (PE) of the **considered target platforms** without being split, which includes *implicit* **dependency** to the considered target platforms.

One of the most critical aspects is to determine a list of BSIs with **appropriate decomposition granularity**, which is strongly influenced by the **diversity of platforms** to be addressed. The main **driver for coarse grain** decomposition is to **keep low the number of BSIs** and the **associated interfaces**, while the main adverse driver, for **fine grain BSIs**, is to have a collection fine-enough BSIs that can accommodate a **large variety of mapping choices**.

The ESSOR methodology implies specification of consistent sets of BSIs that make up the layer application, enabling multiple software implementations

and mapping choices to be realized without breaking consistency of the overall design.

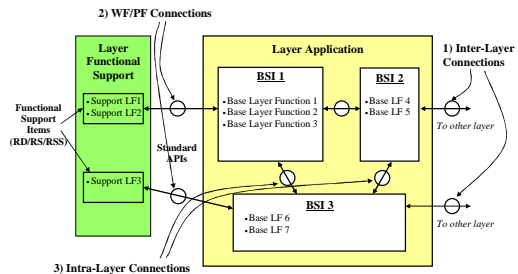Fig. 4 illustrates the outcome of **Base WF partitioning**:

Fig. 4. Illustrative outcome of Base WF Partitioning

3.2.3 Base WF mapping

The entry point of this activity is the set **of BSIs** as identified by previous activity.

The purpose of **Base WF mapping** is to choose the programming language(s), denoted as **target language(s),** that is to /are be used for software implementation of each BSI. Several *target languages* can be considered for a given BSI, for instance C and VHDL (the concerned BSIs being denoted as "**dual BSIs**").

3.3. Base WF Software Design

Base Waveform Software Design is the **second** phase of Base WF development. It consists in designing the **reference software implementation** of the **BSIs**, for the **target language(s)** selected by base WF mapping.

3.3.1 Scope of the software design

A target component is assumed to decompose into: (i) one to many **Workers**, in charge to execute the **functional processing** of the implemented BSIs **strictly independently** from the available **execution environment (configuration and deployment (**SCA 2.2.2 Core Framework (CF)), Operating System (OS) Application Environment Profile (AEP) and connectivity (i.e. CORBA [13] from OMG [14] and MHAL [15])); (ii) the **Container**, in charge to support **Worker(s)** execution in ensuring, **based on** the available **execution environment**, **Worker(s)'** deployment & configuration, connection to other Worker(s) and real-time software scheduling (not needed for FPGAs).

Based on previous definition, the **base WF software design** is dedicated to the **Workers** of the **BSIs** that are developed as **reference porting basis** called **Golden Sources**.

Golden Sources are assigned the **functional requirements** of the implemented BSI. Additionally, **implementation requirements** are assigned in the form of **critical resources implementation budgets** (such as memory usage, cycles count, DMIPS, CLB usage…). **Processing elements** typical of possible target platforms are referenced for expression of the assigned budgets, enabling verification of the assigned requirements in using the Golden Source of selected PEs.

Design of **Golden Sources** can be supported by software engineering models derived from the BSI models, in application of Model Driven Engineering (MDE) principles.

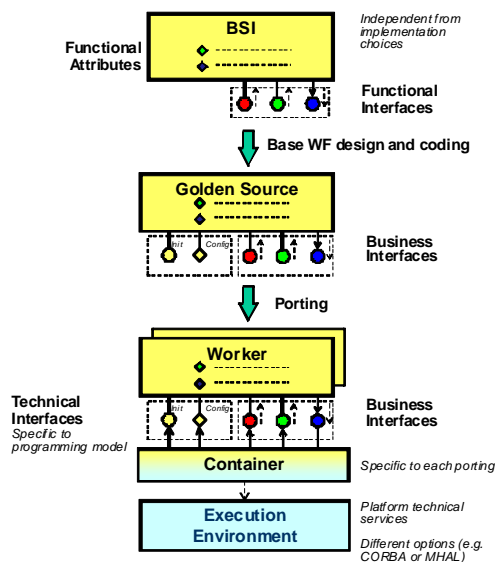Fig. 5 illustrates the aforementioned concepts:

Fig. 5. Chaining of BSI, Golden Source and Worker(s)

3.3.3 Vision of porting

Based on the previous definitions, porting is seen as essentially implying two activities: (i) development of the required **Container**, (ii) integration with the Base WF **Golden Source(s)** and the Target Platform **Execution Environments** (like. SCA 2.2.2 CF, OS and connectivity);.

Usage of **formal IDL characterization of Worker interfaces** and usage of **standard-compliant Execution Environments**, the Container development can be assisted by code generation tools, e.g. in the case of a CORBA broker. Usage of automated code generation is nevertheless **not an obligation**. The **IDL Profiles** defined by the ESSOR Architecture for physical layer components are facilitating automation of Container generation for DSP and FPGA.

Worker of the **target component** is the product of **Golden Source** porting. Execution optimizations can take place as required during the porting (e.g. usage of dedicated libraries or hardware accelerators). When processing power is sufficient, no porting modification is required.

The Golden Source, Worker and Container concepts enable to optimally distribute portability expectations and duties between the Golden Source, that can be entirely reused when porting, and the Container, that is adjusted to each of the porting configurations with potential use of automated code generation. The methodology is therefore featuring "PSM-neutral" / "Configuration Deployment and Connectivity -agnostic" design approach.

In that sense, the Base WF Golden Source is resilient to the evolutions of the SCA standard.

3.4 Base WF Software Coding

Base WF Software Coding consists in developing the Golden Source based on previous design.

The ESSOR Methodology defines **coding rules** derived from JSF program [11], with a specific set defined for C, C++ and VHDL languages. In addition, specific **programming models** are defined to clarify the software interfaces applicable between **Workers** and **Containers** for each of the aforementioned target languages.

3.5 Base WF Native Validation

Usage of a Native Test Environment (NTE) is recommended by the methodology in order to perform an **exhaustive functional validation** of the developed Golden Sources, that are **integrated** and **jointly executed** in order to verify consistency of development and achieved functionalities.

Since aimed at validating the Golden Source, the test applications used within NTE are structured in conformance with the Worker / Container separation principles, with realization of **Native Container**. In the most integrated steps of native validation, the test application can implement complete important parts of the waveform application, justifying usage of **Native Waveform** terminology.

When execution environment of the **Native Test Environment** and the **Target Platform** are close (e.g. in some GPP cases), the Native Waveform as a whole can be considered as a porting basis, therefore increasing the overall level of portability.

4. ESSOR HDR BASE WF DEFINITION

This section presents the way the ESSOR Methodology (§ 3) is applied for developing the HDR Base WF. Reference structure of the HDR Base WF is detailed along with the needed ESSOR Architecture functional support items, considering the application of Common Criteria [12] assurance requirements for security related aspects.

4.1. ESSOR Architecture Functional Support Items

In order to perform its functions, the HDR Base WF relies on ESSOR Architecture to provide the following set of functional support items (RD, RS, RSS APIs):
- *Timing framework:* Used for synchronizing events among different processing elements (PE), and between different nodes.
- *Security framework:* Used for implementing NETSEC, COMSEC and TRANSEC security mechanisms
- *Transceiver framework:* Required to control the access to the wireless channel.
- *SNMP framework:* Used for providing SNMPv3 interface for remote monitoring and control.
- *HMI framework:* Used for providing a HMI for local monitoring and control purpose.
- *IP framework:* Used for accessing the Operating System TCP/IP stack to allow IPv4 simultaneous unicast, multicast and broadcast communications.
- *Event and Log frameworks:* Used for reporting and logging events and SW errors.

4.2. HDR Base WF Reference Structure – PHY Layer

The PHY Layer application is divided in a set of BSIs with the objective of maximizing the portability of the application to the heterogeneous set of platforms available. The BSI decomposition is driven by the following principles:
- *Granularity:* It *s*hould be flexible enough to be adapted to the six different platforms which have different processing architectures (DSP and FPGA based).
- *Functionality:* Resulting BSIs should perform functionally coherent PHY Layer functions. Three main groups of BSIs are identified: Tx Chain, Rx Chain and Common BSIs.
- *Processing requirements:* Monolithic BSIs requiring high processing requirements should be avoided to provide flexibility on the porting stage to different processing architectures.
- *Real-time considerations:* Resulting BSIs should consider its real-time execution. This requires that BSIs should work in a pipelining design, should be independent in its execution, etc.

Applying the above principles, the PHY Layer is partitioned into 16 BSIs with the following functional distribution:
- *4x BSI in the Tx chain:* Responsible of modulation, channel encoding and spectral shaping.
- *8x BSI in the Rx chain:* Responsible of synchronization, equalization, demodulation and channel decoding.
- *4x BSI common to Tx/Rx:* Responsible of the TRANSEC mechanisms, management and control.

When selecting the implementation target for each BSI, there is a need to analyze the different processing architectures of the target platforms, so that the resulting Base WF implementation of the PHY layer is compatible with the mappings (i.e. BSI allocation to a DSP or FPGA processing element) of the six different platforms. Due to the heterogeneous architectures present in the six platforms, some BSIs are implemented for both DSP and FPGA, allowing each NC to choose the most appropriate mapping for its platform. It is worth noting that even if a BSI has two different implementations, it uses the same interfaces with the rest of BSIs and provide the same functionality.

TABLE II summaries PHY Layer partitioning and mapping, where the major number of BSIs is in the Rx chain, which is the most complex part of the design

TABLE II. HDR Base WF PHY Layer decomposition

PHY Layer BSIs	DSP only BSIs	FPGA only BSIs	Dual BSIs (FPGA & DSP)
Tx Chain	2	1	1
Rx Chain	1	1	6
Common	1	-	3

4.3. HDR Base WF Reference Structure – PROT Layers

Protocol layers application is decomposed into 17 BSIs for implementation on multiple GPP as shown in TABLE III.

TABLE III. HDR Base WF Protocol Layers decomposition

PROT Layer	Nb. of BSIs	Red / Black GPP
MAC	6	Black GPP
LLC	3	Black GPP
NET	5	Red / Black GPP
MGT	3	Red GPP

The following principles drive the BSI decomposition:
- *Granularity*: the number of BSI is minimized by considering the execution capacity needs of a Golden Source related to a certain BSI and an easy distribution of BSIs among the available Processing Elements of six

different platforms (by considering a Full Black or Red/Black Deployment).

- *Localized & Independent Execution:* each BSI is designed to group Layer functions that are functionally contiguous and executable independently from the other waveform BSI. This also allows testing the BSI functionalities without any change in the BSI code.
- *Red/Black Exclusivity:* a given BSI may never be designed so that its Golden Source implementation would have one part executing on Red side while another would execute on Black side.
- *Classification isolation:* a given BSI includes the classified parts of the required treatments, in order to minimize the scope of classified software.

The BSI Golden Source is mostly hand written and re-uses the algorithms validated during the HiFi Simulations [6].

The BSI Golden Source validation on NTE requires execution of each single Golden Source in a single Container. NTE Containers are not entirely hand written and take benefit of automated code generation tools usage.

The size of the Golden Source code and the associated Containers on NTE is given in TABLE IV.

TABLE IV. HDR Base WF Protocol Layers size

PROT Layers	Number of BSIs	Golden Source size	Containers expected size
MAC, LLC, NET MGT	17	230 KSLoC(*)	140 KSLoC

(*) SLoC: Source Line of Code

5. ESSOR HDR BASE WF VALIDATION

Verification of the HDR Base WF Golden Source on Native Test Environment (NTE) is decomposed in four levels:
- Level 1: BSI verification.
- Level 2: BSI integration and Layer Validation.
- Level 3: Protocol Layers integration and validation.
- Level 4: Protocol Layers + PHY Layer integration.

Level 1 and 2 cover all Software Requirement Specification (SRS) and implicitly some System Sub-system Specification (SSS) and Security Target (ST) requirements. Level 3 and 4 complete the coverage of SSS and ST requirements.

5.1. Native Test Environment (NTE) Concepts

The NTE is a generic functional test framework designed for all steps related to integration and validation processes of the HDR Base WF, and possibly other waveforms compliant with the ESSOR Architecture, in compliance with the ESSOR Methodology for Portability. NTE allows: i) to create, execute and monitor test cases; ii) to record the simulation scenarios and allow replication of them.

NTE emulates the SDR platform SCA 2.2.2 middleware (i.e. CF and OS) and connectivity (i.e. CORBA and MHAL), and includes the ESSOR Architecture interfaces for WF access to platform resources (RD, RS, RSS).

NTE is composed of PROT-NTE (for validating HDR Base WF protocol layers) and PHY-NTE (for validating HDR Base WF Physical layer). PROT-NTE and PHY-NTE are interconnected together to perform system level verifications of integrated HDR Base WF stack.
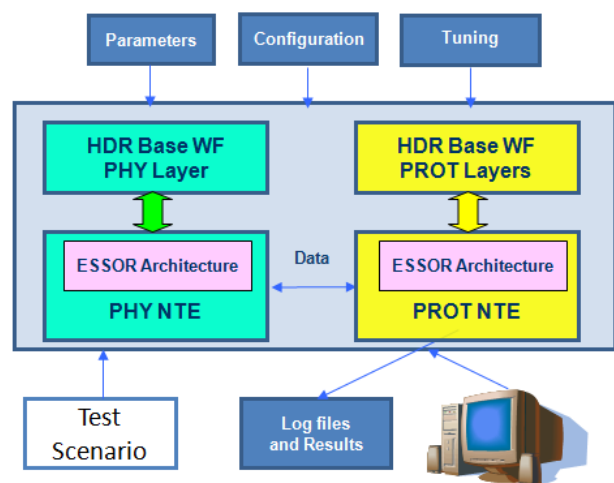

Fig. 6.   Native Test Environment Concepts

5.2. Protocol Native Test Environment (PROT-NTE)

PROT-NTE is a software environment run on LINUX PC machine, which is used during all HDR Base WF Protocol Layers SW validation and integration activities.

PROT-NTE offers the capability to simulate and interconnect several SDR nodes (TR) via simulated physical layer and radio channels, what allows performing all validation and integration activities for the entire HDR Base WF protocol software (NET, LLC, MAC, MGT). It is capable to simultaneous execution up to 24 TRs with full HDR Protocol Stack software (executed on 3 PC machines interconnected via LAN), what allows to perform even scenarios for 24 Nodes network.

PROT-NTE allows to work in Interactive (Scenarios definition, recording and interactive scenarios execution/ replaying) and Batch (automated scenarios execution and replaying e.g. in continues integration process) modes. It emulates „User Services" as different Unicast / Multicast /

Broadcast IP Traffic with configured QoS (e.g. VoIP, routing protocols), SNMP V3 or user data exchange (e.g. files, images), and allows to interact simulated Radio Node with „real" IP Networks.
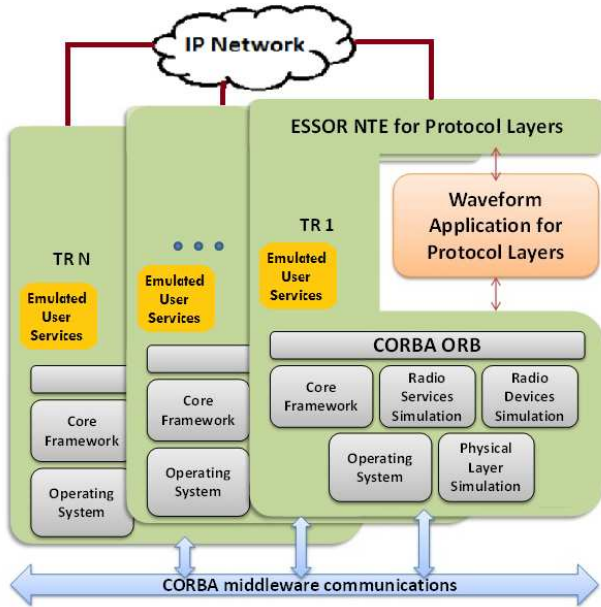

Fig. 7.   Protocol Native Test Environment

5.3. Physical Native Test Environment (PHY-NTE)

PHY-NTE is a generic functional test framework that allows the verification of the HDR Base WF PHY Layer source code SW/FW (targeted for DSP and FPGA devices). In conjunction with the PROT-NTE, it allows the functional verification of the complete HDR Base WF.

PHY-NTE is able to create, execute and monitor test cases for PHY Layer providing up to two nodes simulation (one transmitter and one receiver). PHY NTE runs in "Interactive mode", where user inputs command through the terminal command line, or in "Connected Mode" alongside with PROT-NTE. Test execution can also be automated for batch mode operation without user intervention.

PHY-NTE SW is made of a Testing Framework, ESSOR Architecture Services and Devices emulation (e.g: Transceiver Device, Timing Service…), and a configurable and selectable AWGN radio channel simulation.

PHY-NTE HW is made of COTS DSP and FPGA devices where PHY Layer SW/FW runs, and a LINUX PC Work Station that hosts the SW Testing Framework, the ESSOR Architecture Radio Services and Devices and AWGN radio channel simulation. The communication between devices is achieved by an emulated MHAL like middleware.
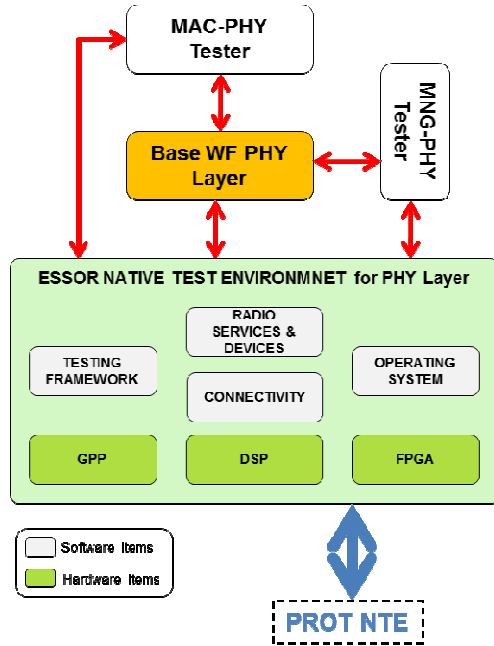

Fig. 8.   Physical Native Test Environment

5.4. Protocol Layers Base WF Test Scenarios

Validation of the HDR Base WF Protocol covers Level 1 to Level 3, fully exploiting the capabilities of PROT-NTE:
- Level 1: BSI validation in a mono node configuration.
- Level 2: Layer integration and validation (several BSIs) in mono/multi nodes configuration
- Level 3: Protocol Layers integration and validation in multi nodes configuration.

Each of those levels contributes in validating Protocol Golden Source behavior within an increasingly large scale of integration, up to entire Protocol Layers working together. Complex scenarios with mobility and dynamic propagation conditions are set up, where the radio transmission between nodes is simulated by the PROT-NTE.

TABLE V gives the number of L1 and L2 tests performed, along with the maximum number of nodes activated.

TABLE V. HDR BASE WF LEVELS 1 AND 2 TESTS

Layer	Levels	Nb. of Tests	Nb. of Nodes
MAC	L1 & L2	597	Up to 24
LLC	L1 & L2	106	Up to 4
NET	L1 & L2	307	Up to 8
MGT	L1 & L2	89	Up to 8
PHY	L1 & L2	294	Up to 2

In order to facilitate the Level 3 integration, a strategy has been adopted that integrates the Protocol Layers in the following functional incremental approach:

- Step 1 (focus on the WF Setup):
  Protocol Layers are loaded on PROT-NTE and the WF is configured and started in a mono node configuration. The simulated SNMP Service is used for testing the basic management activities (e.g. setting/getting of WF parameters, monitoring of WF events).

- Step 2 (focus on the WF Synchronization):
  MAC Layer synchronization between nodes is tested. In order to not introduce complexity to the test, the NET signaling and then the LLC activities are locked.

- Step 3 (focus on the WF Network Creation):
  NET Layer is unlocked, and the network creation and maintenance is tested. LLC functionalities related with NET broadcast signaling transmission are also checked.

- Step 4 (focus on the WF Data Transmission):
  IP Traffic (unicast, multicast and broadcast) is injected using the PROT-NTE IP Service. LLC functionalities related with IP Traffic transmission, priority queues handling and network congestion are also checked.

Once the Protocol layers have been successfully integrated, an incremental approach has been adopted to progressively validate the functionalities and performance, moving from small / medium network size to bigger network size. The main steps for the Protocol validation are:

a) Validation with network size up to 8 nodes:

This intermediate step validates HDR Base WF Protocol in networks of up to 8 nodes as shown in TABLE VI.

TABLE VI. VALIDATION STATISTICS UP TO 8 NODES

Functionalities/ Performance Measurements	Test Nbr
• Reading/Writing of WF parameters • MAC Synchronization (with/without GNSS) • Network Topology Management • IP transmission (Unicast/Multicast/Broadcast) • Optimized Multicast/ Broadcast Transmission • Network Congestion Management Emergency Message Handling	44

b) Validation with network size up to 24 nodes:

This step validates the full HDR Base WF Protocol in networks of up to 24 nodes as shown in TABLE VII.

TABLE VII. VALIDATION STATISTICS UP TO 24 NODES

Functionalities/ Performance Measurements	Test Nbr
• MAC Synchronization (all nodes without GNSS) • Networks Splitting and Merging • Enhanced MAC Algorithms (PDN, DTA, TC, …) • Security Key Management • ARQ Handling VOIP Support	34

5.5. Physical layer Base WF Test Scenarios

PHY Base WF verification (TABLE V) covers L1 and L2 levels, using the PHY-NTE capabilities. Additionally the development environment is used for some L1 test cases.

- *Level 1: BSI verification tests.* PHY Layer BSIs are validated internally (white-box approach using the development environment) and at interface level (black-box approach using the PHY-NTE).
- *Level 2: Integrated PHY Layer verification tests.* The PHY Layer is integrally verified at interface level, with all the BSIs integrated (black-box approach). Tests are performed with single node and with two nodes. In that case, Tx / Rx communication are verified, using AWGN channel simulation provided by PHY-NTE.

The test scenarios run on the PHY-NTE require:
- Specific PHY-NTE configuration.
- Testers, which simulate the interface functions, i.e. the behavior of other BSIs, layers and PTF components.
- Test vectors, containing data for input and/or output.

The last element of the testing framework is the floating-point and fixed-point models of the PHY Layer created on SIMULINK (MATLAB) [16] as described in [6]. The models serve the following purposes:
- Fixed-point model validation in comparison with the floating-point model.
- Generation of test vectors, which are used as input and/or output data for the test cases (L1 & L2).
- Verification of the test cases results. The output vector of the test case and the output vector of the SIMULINK fixed-point model are compared (L1 & L2).

The advantage of performing the porting based on the BSI partitioning is that the same test vectors can be used for the verification of the target implementation of each BSI.

5.6. Base WF Level 4 (L4) Test Scenarios

Integrated HDR Base WF (PHY and Protocol layers) is verified using the interconnected PHY-NTE and PROT-NTE. L4 verification (organized around 12 scenarios) covers 2-node Base WF configuration and adaptive interaction between PHY and Protocol layers.

6. ESSOR HDR BASE WF PORTING ON HETEROGENOUS SDR PLATFORMS

6.1. Incremental Porting Activities

The HDR Base WF is currently ported on five (5)[1] different heterogeneous ESSOR National SDR PTFs where ESSOR Architecture has already been implemented. Details about these SDR PTFs are provided in [6].

The HDR Base WF software porting into national SDR PTFs is also using incremental approach following the rhythm of Base WF incremental testing. In each step a number of new functionalities are included into waveform (release). Such a release is ported into each PTF, the tests which are defined for each steps are performed nationally by all developers. After that, interoperability testing between different implementations (PTFs) is conducted but including the test vectors exchange (offline) between PTFs in advance in order to be sure that all the parameterization is inline. By this way the final interoperability testing with full capabilities and test scenarios is better secured.

At the time of writing this paper, initial point to point interoperability tests have been conducted successfully, demonstrating that different ESSOR National SDR platforms can communicate over the air interface.

6.2. Initial Lessons Learnt

The method used to develop and port HDRWF is showing its benefits. The different levels of simulation have been given confidence for technical decision made and about performance (requirements) which should be achieved. Simulations have also provided common supporting information (e.g in form of test vectors) for validating on a common basis the outputs of the National porting phases performed in parallel by the various NC. Using NTE for Base WF testing and validation gives confidence for correct functionality of golden source code and so allow developers to concentrate on Target PTF issues (like performance) during porting phase. Using common code in parallel of National porting activities also provide faster feedback for Base WF developers and testing in form of change requests or bug reports as there is more work force working with software same time.

7. CONCLUSIONS AND FURTHER STEPS

This paper presents the current achievements of the ESSOR Programme in defining the ESSOR Methodology for WF Portability. This methodology is promoting a "Configuration, Deployment and Connectivity agnostic" design approach and is applied to the development of the HDR Base WF Golden Source, the common portable software jointly developed by the ESSOR NCs. In that sense, the HDR Base WF complies with the WF functional requirements and is resilient to the evolutions of the SCA standard.

After providing an overview of the capabilities of the HDRWF, this paper details about design and validation of the HDR Base WF, along with the initial lessons learnt from incremental National porting activities.

The ESSOR Programme is a successful example of joint development between different Nations and Industries in a high cooperative manner for coalition purposes. The HDRWF is aimed at becoming operational and the ESSOR Participating States intend to have the HDRWF adopted in the Coalition Wideband Networking Waveform (COALWNW) program and as a standard for the European Community and NATO.

In parallel of these developments, future phase of the ESSOR Programme is being initiated and is addressing for the ESSOR products (ESSOR Architecture, ESSOR HDRWF): i) standardization and certification; ii) technical enhancements; iii) support to operational deployment.

8. REFERENCES

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[1] For budgetary constraints, Sweden has limited its national activities to the implementation of ESSOR Architecture into its own National Platform.